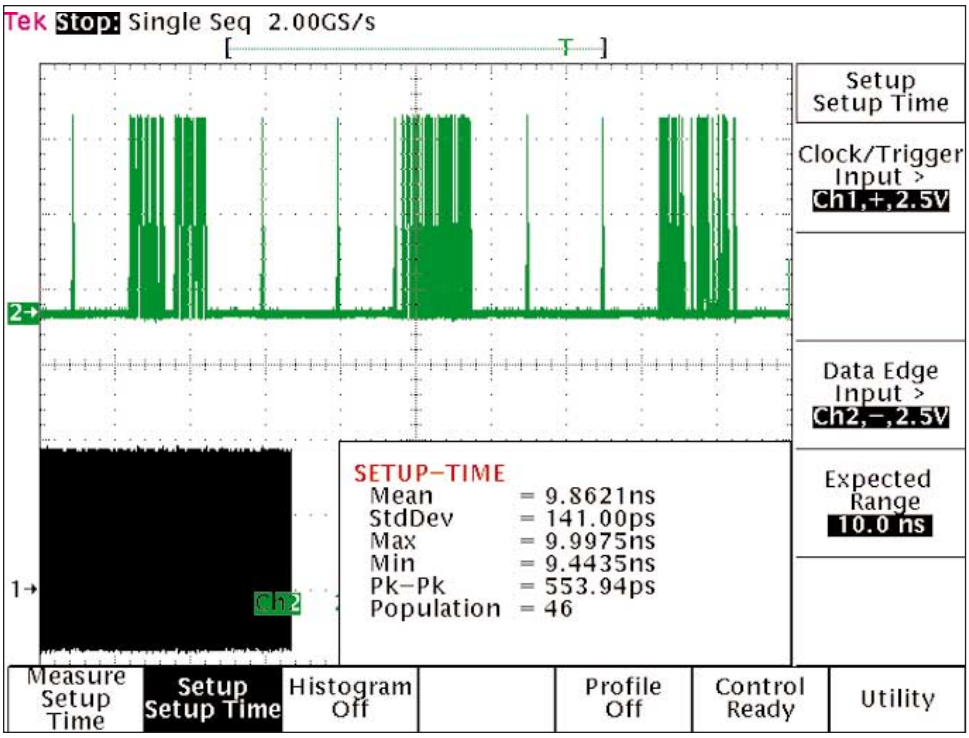
Tektronix

Application Note

New Timing Measurement Techniques for High Speed Processors using TDS Oscilloscopes



TDSPSM1 collecting timing statistics from user-defined clock edges to user-defined data edges.

Introduction

With rapidly ascending processor clock rates and tighter timing considerations comes a more pressing need to precisely determine timing margins. Traditional timing measurements, which use cursors or histograms to make statistical determinations of timing, have been limited by their inability to directly correlate a particular clock edge to the corresponding data edge. In addition, these techniques have not been able to characterize specific data transitions.

Today's high bandwidth acquisition circuits, extremely long record lengths, and custom SW applications are making possible a new level of precision in timing measurements. This application note will use the most common timing measurement, setup-and-hold timing, to illustrate this new capability. We will start with a traditional setup time measurement – which uses multiple triggered acquisitions to acquire timing data – then compare it with the new timing capability – which captures all timing data in a single acquisition. Then we'll discuss the advantages of the new capability.

Traditional Setup Time Measurement

Figure 1 shows the output of a Tektronix oscilloscope performing a typical processor setup time measurement. For this measurement, Channel 1 is clock and Channel 2 is data. The oscilloscope's infinite persistence mode was used to capture the data, and cursors are used to determine the minimal setup time.

From this illustration, you can see how difficult it is to precisely measure setup timing with histograms and cursors. Parameters such as trigger jitter and vertical noise can cause both the clock and data waveforms to shift horizontally in time. As a result, the right-most data transition is probably not acquired at the same time as the left-most clock transition. The minimum setup time of 400 ps measured with the cursors does not truly show the margin available. Note:

- The scattering of points on the data channel
- The positive and negative data transitions have different setup time margins
- The oscilloscope is in equivalent time mode (it's capturing data over multiple trigger acquisitions)

A New Way To Make Timing Measurements

In Figure 2, the Tektronix TDS694C oscilloscope equipped with the new Tektronix TDSPSM1 Processor Specifications Measurements package performs a setup time measurement. The measurement summary shows that 119 valid data-to-clock timing measurements were performed on a single 250,000 point acquisition. The setup time measurements have a minimum margin of 7.2966 ns with a standard deviation of 667.39 ps.

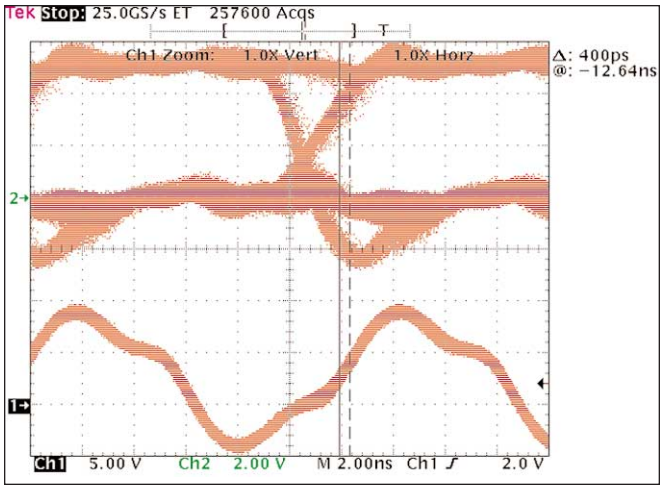


Figure 1. Measuring setup time with cursors.

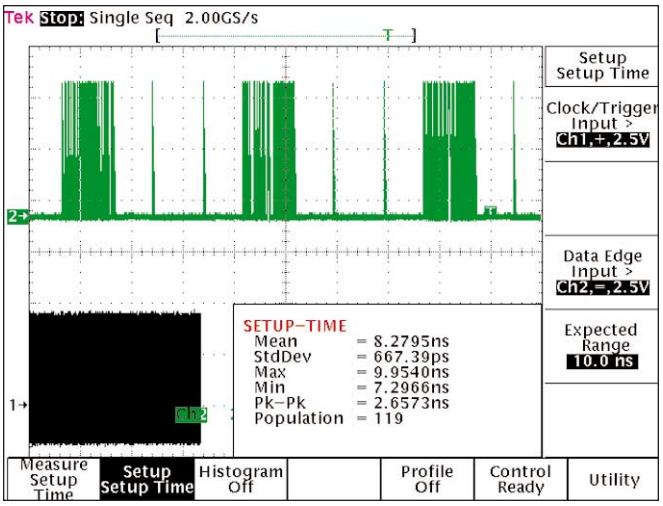


Figure 2. Setup time measurement with new timing measurement technique.

How Is This New Technique Different?

The traditional cursor and histogram measurement techniques are performed over multiple triggered acquisitions as shown in Figure 3.

With traditional timing measurements, information about specific margins is confounded by the nature of the acquisition. Trigger jitter of the scope influences the acquisitions and can appear to reduce the true margin.

The new timing measurement technique, performed by the Tektronix TDSPSM1 application package, measures timing on each and every valid edge in an acquisition waveform whose length can range from 500 to 8 million points (Figure 4). In addition, the 10 GS/s sample rate and 3 GHz bandwidth of the TDS694C allows single-shot viewing of high speed digital signals at high resolution.

This allows true one-to-one correlation between a specific clock edge and its corresponding data transition.

Another advantage of this new capability is that the user can collect information about specific edges. In Figure 1, timing information is collected on both data edge transitions. As can be seen,

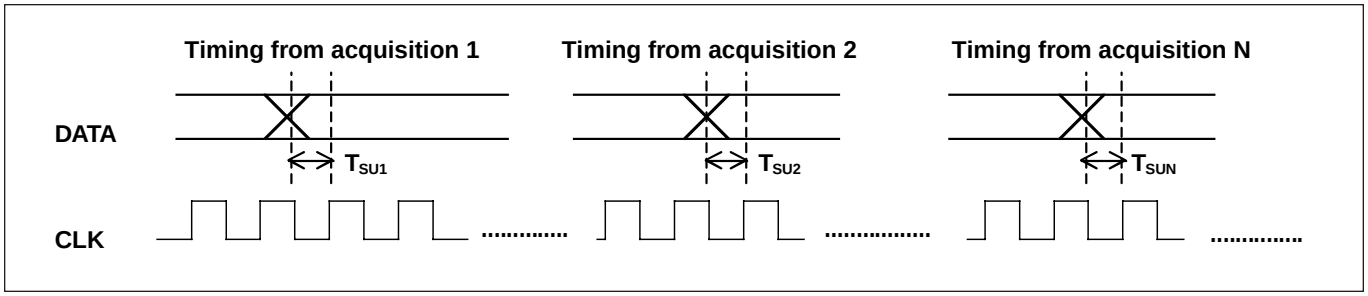


Figure 3. Multiple triggered acquisitions.

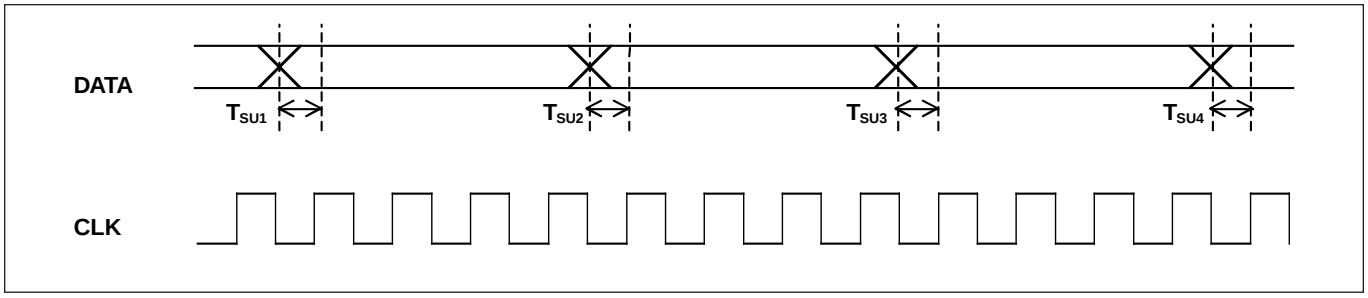


Figure 4. All valid edges from a single-triggered acquisition.

the setup time budget varies depending upon whether the data is going positive or negative. Figure 5 shows the TDSPSM1 measurement of set-up timing information for 46 valid edges that transition from positive to negative. The TDSPSM1 application package is designed to be versatile so that it can collect statistics from user-defined clock edges to user-defined data edges.

The setup and hold timing measurements described above have many components that comprise the data valid window. These components include rise, fall, low, and high times. Figure 6 shows these critical measurements made on approximately 2,300 valid cycles. Again, what is significant about these measurements is that they were made on each and every valid cycle in a single-shot acquisition. For example, the max rise-time parameter tells you the worse case rise-time out of the 2,340 rise-times that were captured with single-shot acquisitions.

Conclusion

With the Tektronix TDS Digital Oscilloscopes and the new TDSPSM1 application package, Tektronix introduces a way to make more precise timing measurements. By combining the new TDSPSM1 measurement technique with TDS500D/600C/-700D Digital Oscilloscopes that provide sample rates to 10 GS/s, bandwidths to 3 GHz, and record lengths to 8 MB, customers can make timing measurements of unprecedented accuracy from single-triggered acquisitions.

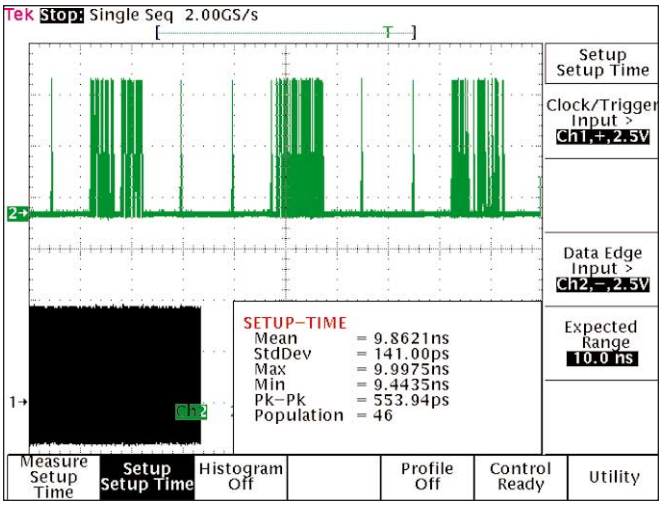


Figure 5. Setup time measurement with specific setups.

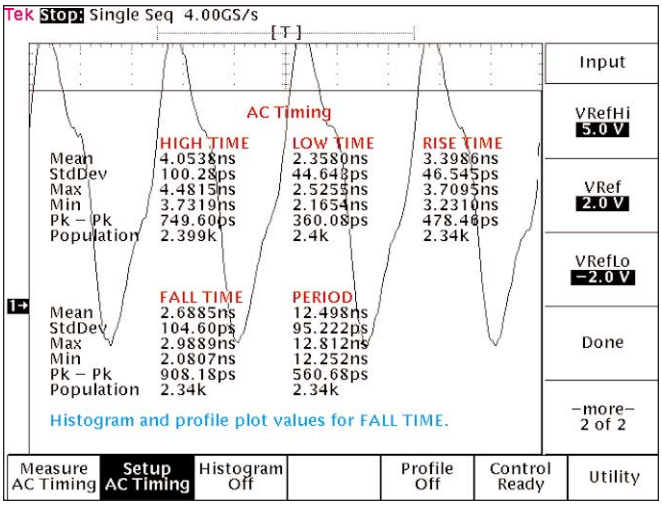


Figure 6. Setup timing over 2300 cycles.

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